CLAIMS

What is Claimed is:

1. A semiconductor device that has a structure in which a semiconductor chip includes a first conductor member, a second conductor member provided with a dielectric interposed between the first conductor member and the second conductor member, a third conductor member provided with a dielectric interposed between each of the first and second conductor members and the third conductor member, and a capacitance measuring circuit, wherein

the capacitance measuring circuit comprises:

a charging voltage supply part for charging the first conductor member, said charging voltage supply part being connected via a first charge-side switching transistor to the first conductor member;

a current sampling part for sampling currents flowing through the second and third conductor members, said current sampling part being connected via first and second switching transistors for measuring current to the second and third conductor members, respectively; and

a control circuit for controlling ON/OFF switching of each of the switching transistors, and

the second conductor member is connected to the charging voltage supply part via a second charge-side switching transistor whose ON/OFF switching is controllable by the control circuit.

2. The semiconductor device of Claim 1, wherein

the third conductor member is connected via a third charge-side switching transistor to the charging voltage supply part, and

the first conductor member is connected via a third switching transistor for measuring current to the current sampling part.

3. The semiconductor device of Claim 2, wherein

a switching transistor for decreasing off-leakage current is placed between each of the first through third conductor members and the current sampling part, said switching transistor being connected in series with a corresponding one of the first through third switching transistors for measuring current and having a higher threshold voltage than said corresponding switching transistor for measuring current.

4. The semiconductor device of Claim 3, wherein

each of the switching transistors for decreasing off-leakage current is controlled by a gate bias common with the switching transistor for measuring current connected in series with the switching transistors for decreasing off-leakage current.

5. The semiconductor device of Claim 2, wherein the semiconductor device further comprises a discharge part, and

the first through third conductor members are connected to the discharge part via first through third discharge-side switching transistors, respectively.

6. The semiconductor device of Claim 5, wherein:

the first charge-side switching transistor and the first discharge-side switching transistor are a PMISFET and an NMISFET the drains of which are connected to each other, said common drains being connected to the first conductor member;

the second charge-side switching transistor and the second discharge-side switching transistor are a PMISFET and an NMISFET the drains of which are connected to each other, said common drains being connected to the second conductor member; and

the third charge-side switching transistor and the third discharge-side switching transistor are a PMISFET and an NMISFET the drains of which are connected to each other, said common drains being connected to the third conductor member.

7. The semiconductor device of Claim 6, wherein

in a mode for measuring the capacitance between any two of the first through third conductor members, the control circuit holds the discharge-side switching transistor connected to the other conductor member whose current is not to be measured in the ON

state.

8. The semiconductor device of Claim 1, wherein

the first through third conductor members are all interconnects.

9. The semiconductor device of Claim 1, wherein

the first through third conductor members are any three-way combination of a source/drain region, a substrate region and a gate electrode of a MISFET.

10. The semiconductor device of Claim 9, wherein

the MISFET is an NMISFET, and

the substrate region is a P-well located in the uppermost position of a triple well.

11. The semiconductor device of Claim 1, wherein the semiconductor device comprises a fourth conductor member in addition to the three conductor members, and

in the capacitance measuring circuit, the fourth conductor member is connected via a fourth charge-side switching transistor to the charging voltage supply part and via a fourth switching transistor for measuring current to the current sampling part.

12. The semiconductor device of Claim 1, wherein

the charging voltage supply part operates at a power supply voltage lower than that supplied to the control circuit.

13. The semiconductor device of Claim 1, wherein:

the capacitance measuring circuit comprises an oscillator for generating a clock signal having a higher frequency than an external clock signal; and

the control circuit operates on the basis of the clock signal output from the oscillator.

14. The semiconductor device of Claim 13, wherein

the capacitance measuring circuit comprises a frequency divider for dividing the frequency of the clock signal output from the oscillator.